UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/591,910	07/21/2008	Sei Yang Yang	043946-4	3398

25570 7590 09/16/2009

ROBERTS MLOTKOWSKI SAFRAN & COLE, P.C.
Intellectual Property Department
P.O. Box 10064
MCLEAN, VA 22102-8064

EXAMINER	
CHAD, ANISS	

ART UNIT	PAPER NUMBER
4191	

NOTIFICATION DATE	DELIVERY MODE
09/16/2009	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

lgallaugher@rmsclaw.com
dbeltran@rmsclaw.com
bdiaz@rmsclaw.com

Office Action Summary	Application No.	Applicant(s)	
	10/591,910	YANG, SEI YANG	
	Examiner	Art Unit	
	ANISS CHAD	4191	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 September 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *122-145* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *122-145* is/are rejected.

7)☒ Claim(s) *122-127, 129-138, 140* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 September 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *10/08/2008*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Status

Claims 1-145 are pending in the instant application.

Claims 1-121 are canceled and claims 122-145 are added by a preliminary amendment filed on 09/07/2006.

Claims 122-145 stand rejected.

Information Disclosure Statement

The information disclosure statement (IDS) submission on 10/08/2008 is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Claim Objections

Claims 122-127, 129-138, 140 are objected to because there is insufficient antecedent basis in the following limitations:

"the design code", claim 122, line 3, claim 123, line 2, claim 124, line 2, claim 125, line 2, claim 126, line 2, claim 129, line 3, claim 130, line 2, claim 133, line 3, claim 134, line 2, claim 135, line 7, claim 136, line 3, and claim 137, line 3.

"the design net-list", claim 122, line 3, claim 123, line 2, claim 124, line 2, claim 125, line 2, claim 126, line 2, claim 129, line 3, claim 130, line 2, claim 133, line 3, claim 134, line 2, claim 135, line 7, claim 136, line 3, and claim 137, line 3.

"the necessary information", claim 122, claim 126, line 7, claim 129, line 4, claim 130, line 8, claim 133, line 4, claim 134, line 8, claim 135, line 7.

"the minimally necessary information", claim 123, line 7, claim 124, line 7.

"the back-stage simulation", claim 122, line 5, claim 123, line 9, claim 124, line 9, claim 125, line 8, claim 126, line 8, claim 129, line 5, claim 130, line 9, claim 133, line 5, claim 134, line 6, claim 124, line 9, claim 135, line 5.

"the 1st simulation run", claim 122, line 7, claim 123, line 4, claim 124, line 4, claim 126, line 4, claim 129, line 7, claim 130, line 4, claim 133, line 7, claim 134, line 5, claim 135, line 4, claim 136, line 3, and claim 137, line 3.

"the front-stage simulation", claim 122, line 7, claim 123, line 11, claim 124, line 11, claim 125, line 7, claim 126, line 11, claim 129, line 7, claim 130, line 11, claim 135, line 5.

"The design verification method", claim 127, line 1, claim 137, line 1, claim 132, line 1.

"the additional code", claim 133, line 3.

"the verification run", claim 139, line 1, claim 140, line 1, claim 142, line 1.

"the detection method", claim 138, line 1.

Claim 138 is objected to because of the following informalities:

Claim 138 states in line 4 "...includesto...", this limitation should read "...includes to...".

Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 122-124, 126, 129-131, 133-135 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The limitation "fast" in claim 122, line 8, claim 123, lines 12, claim 124 line 12, claim 126, line 12, claim 129, line 8, claim 130, line 12, claim 133, line 10, claim 134,

line 14, and claim 135 line is not clear. In addition, the limitation "high" in claim 122, line 9, claim 123, lines 13, claim 124 line 13, claim 126, line 13, claim 129, line 9, and claim 130, line 13 is not clear. These are relative and comparative terms that are unclear and are not defined in the specification, rendering the claims indefinite. The examiner will not give these terms weight in interpreting the claims.

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claims 122, 129, 133, 136 are rejected under 35 U.S.C. 101 because claimed invention is directed to non-statutory subject matter.

As per Claim 122: Claim 122 recites an 'apparatus' comprising of "a verification software…" that constitutes nothing more then software components as evidence by the specification. The specification explicitly mentions "the verification apparatus which uses simulation, and if necessary, formal verification, simulation acceleration, hardware emulation, and(or) prototyping (called a verification platform in a common name) together to increase the efficiency and performance of verification for verifying at least multi-million gate digital designs…".

Accordingly, the recited "design verification apparatus" is **software *per se*** and is not a "process," a "machine," a "manufacture" or a "composition of matter," as defined in 35 U.S.C. 101, and constitutes non-statutory subject matter.

As per Claim 129: Claim 129 recites an 'apparatus' comprising of "a verification software…" that constitutes nothing more then software components as evidence by the specification. The specification explicitly mentions "the verification apparatus which uses simulation, and if necessary, formal verification, simulation acceleration, hardware emulation, and(or) prototyping (called a verification platform in a common name) together to increase the efficiency and performance of verification for verifying at least multi-million gate digital designs…".
Accordingly, the recited "design verification apparatus" is **software *per se*** and is not a "process," a "machine," a "manufacture" or a "composition of matter," as defined in 35 U.S.C. 101, and constitutes non-statutory subject matter.

As per Claim 133: Claim 133 recites an 'apparatus' comprising of "a verification software…" that constitutes nothing more then software components as evidence by the specification. The specification explicitly mentions "the verification apparatus which uses simulation, and if necessary, formal verification, simulation acceleration, hardware emulation, and(or) prototyping (called a verification platform in a common name) together to increase the efficiency and performance of verification for verifying at least multi-million gate digital designs…".
Accordingly, the recited "design verification apparatus" is **software *per se*** and is not a "process," a "machine," a "manufacture" or a "composition of matter," as defined in 35 U.S.C. 101, and constitutes non-statutory subject matter.

As per Claim 136: Claim 136 recites an 'apparatus' comprising of "a verification software…" that constitutes nothing more then software components as evidence by the specification. The specification explicitly mentions "the verification apparatus which uses simulation, and if necessary, formal verification, simulation acceleration, hardware emulation, and(or) prototyping (called a verification platform in a common name) together to increase the efficiency and performance of verification for verifying at least multi-million gate digital designs…".

Accordingly, the recited "design verification apparatus" is **software *per se*** and is not a "process," a "machine," a "manufacture" or a "composition of matter," as defined in 35 U.S.C. 101, and constitutes non-statutory subject matter.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 122-145 are rejected under 35 U.S.C. 102(e) as being anticipated by Rajsuman et al. (US Patent No.: US 6678645 B1) hereinafter Rajsuman.

Regarding claim 122, Rajsuman discloses "a design verification apparatus (Fig. 6, 66) comprising: a verification software (Fig. 2, Col. 5 lines 54-56) and one or more simulators (Fig. 1, 28), wherein the said verification software instruments an additional code or a circuit into the design code (Col. 2, lines 33-35) or into the design net-list (Col.3, lines 18-20) in an automatic way (Fig. 3, EDA (Electronic Design Automation)), so that the necessary information (with which one or more post-1st simulations that run as the back-stage simulation can be executed against one or more design objects in the said design code or in the design net-list) can be collected during the 1st simulation run (Col. 7, lines 4-11), referred to as the front-stage simulation, and the said one or more post-1st simulation runs are executed fast while obtaining the visibility, thereby providing high simulation speed (Col. 3, lines 41-44) or high visibility for debugging".

Regarding claim 123, Rajsuman discloses "a design verification method (Fig. 2, Col. 5 lines 54-56), in which one or more design bugs in the design code or in the design net-list are identified and collected (Col. 11, lines 58-62) by a number of simulation executions with a number of test benches (Fig. 2, S33, S34, Figs .5-9), comprising the following steps: some of said simulation executions are decomposed into the 1st simulation run as the front-stage simulation and the post-1st simulation runs as the back-stage simulation (Fig. 6, 92, Col. 10, lines 15-26); verification software instruments an additional code or a circuit into the design code (Col. 2, lines 33-35) or into the design net-list (Col.3, lines 18-20) in an automatic way (Fig. 3, EDA (Electronic

Design Automation)), so that the minimally necessary information(with which one or more post-1st simulations that run as the back-stage simulation can be executed against one or more design objects in the said design code or in the design net-list) can be collected during the 1st simulation run (Col. 7, lines 4-11) (the front-stage simulation), and said one or more post-1st simulation runs are executed fast while obtaining the visibility, thereby providing fast simulation speed (Col. 3, lines 41-44) or high visibility for debugging" (Col. 11, lines 58-62).

Regarding claim 124, Rajsuman discloses "a design verification method (Fig. 2, Col. 5 lines 54-56), in which one or more design bugs in the design code or in the design net-list are identified and corrected (Col. 11, lines 58-62) by a number of simulation executions with a number of test benches (Fig. 2, S33, S34, Figs. 5-9), implemented as follows: some of the said simulation executions are decomposed into the 1st simulation run as the front-stage simulation and the post-1st simulation runs as the back-stage simulation (Fig.6, 92, Col. 10, lines 15-26); verification software instruments an additional code or a circuit into the design code (Col. 2, lines 33-35) or the design net-list (Col.3, lines 18-20) in an automatic way (Fig. 3, EDA (Electronic Design Automation)), so that the minimally necessary information(with which one or more post-1st simulations that run as the back-stage simulation can be executed against one or more design objects in the said design code or in the design net-list) can be collected during the 1st simulation run (Col. 7, lines 4-11) (the front-stage simulation), and said one or more post-1st simulation runs are executed fast while obtaining the

visibility, thereby providing both fast simulation speed (Col. 3, lines 41-44) and high visibility for debugging" (Col. 11, lines 58-62).

Regarding claim 125, Rajsuman discloses "a design verification method (Fig. 2, Col. 5 lines 54-56), in which one or more design bugs in the design code or in the design net-list (Col.3, lines 18-20) are identified and corrected (Col. 11, lines 58-62) by a number of simulation executions with a number of test benches (Fig. 2, S33, S34, Figs. 5-9), characterized in that the method is composed of the following steps: the design states of one or more design objects in DUV and, in necessary, the design states of one or more design objects in test bench (Figs. 5-9, DVS, Testbench) are saved at one or more simulation times during one or more 1st simulation runs (Figs. 4B, 5, Col. 8, lines 39-44) (the front-stage simulation), and the parallel post-1st simulation runs are executed from the saved design states as the back-stage simulation (Col. 8, lines 58-64).

Regarding claim 126, Rajsuman discloses "a design verification method, in which one or more design bugs in the design code or in the design net-list are identified and corrected by a number of simulation executions with a number of test benches (Fig. 2, S33, S34, Figs. 5-9), comprising the following steps: some of the said simulation executions are decomposed into the 1st simulation run as the front-stage simulation and the post-1st simulation runs as the back-stage simulation (Fig. 6, 92, Col. 10, lines 15-26); verification software instruments an additional code or a circuit into the design code

(Col. 2, lines 33-35) or the design net-list (Col.3, lines 18-20) in an automatic way (Fig. 3, EDA (Electronic Design Automation)) so that the necessary information (with which one or more post-1st simulation runs as the back-stage simulation can be executed against one or more design objects in said design code or in the design net-list) can be collected during the 1st simulation run (Col. 7, lines 4-11) (the front-stage simulation), and the said one or more post-1st simulation runs are executed fast while obtaining the visibility (Col. 3, lines 41-44), thereby providing both fast simulation speed (Col. 3, lines 41-44) and high visibility for debugging" (Col. 11, lines 58-62).

Regarding claim 127, Rajsuman discloses "a design verification method, in which a simulation at the lower level of abstraction is executed rapidly (Col. 2, lines16-22) by using the simulation results from one or more simulation runs at the higher level of abstraction (Col. 2, lines 42-43).

Regarding claim 128, this claim being dependant on claim 127 inherits the rejections of the limitations of that claim. Applicant's attention is directed to the rejection of claim 127. In addition, Rajsuman discloses "a design verification method according to claim 127, wherein:

- one or more simulation runs at the higher level of abstraction is a transaction-level simulation (Fig. 1, 21, Behavioral HDL) and the simulation at the lower level of abstraction is a register transfer-level simulation (Fig. 1, 23, RTL), a gate-level simulation (Fig. 1, 25), a

transaction/register transfer mixed-level simulation, a transaction/gate mixed-level simulation, a register transfer/gate mixed-level simulation, or a transaction/register transfer/gate-level mixed-level simulation; one or more simulation runs at the higher level of abstraction is a register transfer-level simulation (Fig. 1, 23, RTL) and the simulation at the lower level of abstraction is a gate-level simulation (Fig. 1, 25), or a mixed register transfer/gate-level simulation;

- one or more simulation runs at the higher level of abstraction is a simulation based on a simple delay model and the simulation at the lower level of abstraction is a simulation based on a more accurate delay model than the said simple delay model (Col. 11, lines 30-41);
- one or more simulation runs at the higher level of abstraction (Fig. 1, RTL, Col. 3, lines 45-46) is a cycle-based simulation (Col. 3, lines 57-59) and the simulation at the lower level of abstraction is an event-driven simulation (Fig. 1, Physical Design, Col. 9, lines 1-5), or
- the said simulation results from one or more simulation runs at the higher level of abstraction which is used at a simulation at the lower level of abstraction contains either at least design state of one or more design objects so that a simulation at the lower level of abstraction is executed by the temporally parallel execution method or at least one or more input information for replay (Col. 11 lines 14-17), or input/output information for

replay of design objects so that a simulation at the lower level of abstraction is executed by the spatially parallel execution method".

Regarding claim 129, Rajsuman discloses "a design verification apparatus (Title, Abstract) comprising: a verification software and one or more simulators, wherein the said verification software instruments an additional code or a circuit into the design code (Col. 2, lines 33-35) or into the design net-list (Col.3, lines 18-20) in an automatic way (Fig. 3, EDA (Electronic Design Automation)) so that the necessary information (with which one or more post-1st simulation runs as the back-stage simulation can be executed against one or more design objects in the said design code or in the design net-list) can be collected during the 1st simulation run (Col. 7, lines 4-11) (the front-stage simulation), and the said one or more post-1st simulation runs are executed fast while obtaining the visibility, thereby providing both fast simulation speed (Col. 3, lines 41-44) and high visibility for debugging" (Col. 11, lines 58-62).

Regarding claim 130, Rajsuman discloses "a design verification method, in which one or more design bugs in the design code or in the design net-list are identified and collected (Col. 11, lines 58-62) by a number of simulation executions with a number of test benches (Fig. 2, S33, S34, Figs .5-9), comprising the following steps: some of the said simulation executions are decomposed into the 1st simulation run as the front-stage simulation and the post-1st simulation runs as the back-stage simulation (Fig.6, 92, Col. 10, lines 15-26); verification software instruments an additional code or a circuit into the

design code (Col. 2, lines 33-35) or into the design net-list (Col.3, lines 18-20) in an automatic way (Fig. 3, EDA (Electronic Design Automation)) so that the necessary information (with which one or more post-1st simulation runs as the back-stage simulation can be executed against one or more design objects in the said design code or in the net-list) can be collected during the 1st simulation run (Col. 7, lines 4-11), (the front-stage simulation), and the said one or more post-1st simulation runs are executed fast while obtaining the visibility, thereby providing both fast simulation speed (Col. 3, lines 41-44) and high visibility for debugging" (Col. 11, lines 58-62).

Regarding claim 131, Rajsuman discloses "a design verification method, in which there is no change in the design objects, where the minimal simulation results are saved during the run of the front-stage simulation (Col. 10, lines 14-15), the saved simulation results are used for running one or more back-stage simulations either in parallel with two or more simulators or in sequence with a single simulator (Col. 10, line 13, *the address sequencer 88*), and, if necessary, the signal dump for one or more variables or signals in one or more design objects is carried out during the back-stage simulation, thereby achieving high visibility (Col. 9, lines 10-15).

Regarding claim 132, Rajsuman discloses "a design verification method, in which a simulation at the higher level of abstraction is executed in such a way that its simulation result is entirely or partially corrected by using the simulation result from a simulation at the lower level of abstraction" (Col. 11, lines 42-45).

Regarding claim 133, Rajsuman discloses "a design verification apparatus (Title, Abstract) comprising: a verification software (Fig. 2, Col. 5 lines 54-56) and at least two or more different verification platforms (Fig. 1), wherein the said verification software instruments the additional code or circuit into the design code (Col. 2, lines 33-35) or into the net-list (Col.3, lines 18-20) in an automatic way (Fig. 3, EDA (Electronic Design Automation)) so that the necessary information(with which one or more post-1st verification runs as the back-stage verification on the verification platforms among which at least one verification platform is different from the verification platform for the 1st verification run can be executed against one or more design objects in the said design code or net-list) can be collected during the 1st verification run (Col. 7, lines 4-11), which is the front-stage verification, and the said one or more post-1st verification runs are executed fast" (Col. 3, lines 41-44).

Regarding claim 134, Rajsuman discloses "a design verification method, in which one or more design bugs in the design code or in the design net-list are identified and corrected (Col. 11, lines 58-62) by running a number of verification executions using at least two or more verification platforms in a hybrid way (Fig. 1), comprising the following steps: some of the said verification executions are decomposed into the 1st verification run as the front-stage verification and the post-1st verification runs as the back-stage verification (Fig. 6, 92, Col. 10, lines 15-26); an additional code or a circuit is instrumented into the design code (Col. 2, lines 33-35) or the design net-list (Col.3, lines

18-20) in an automatic way (Fig. 3, EDA (Electronic Design Automation)) so that the necessary information (with which one or more post-1st verification runs as the back-stage verification on the verification platforms among which at least one verification platform is different from the verification platform for the 1st verification run can be executed against one or more design objects in the said design code or in the design net-list) can be collected during the 1st simulation run (Col. 7, lines 4-11) (front-stage simulation), and the said one or more post-1st simulation runs are executed fast as they are executed against one or more specific blocks only" (Col. 3, lines 41-44).

Regarding claim 135, Rajsuman discloses "a design verification method, in which an additional verification uses the results from previous execution of an arbitrary simulation (Fig. 7, 76), simulation acceleration, hardware emulation (Fig. 7, 72), or prototyping, comprising the following steps" the said additional verification is decomposed into the 1st verification run as the front-stage verification and the post-1st verification runs as the back-stage verification (Fig. 6, 92, Col. 10, lines 15-26); verification software instruments an additional code or a circuit to in the design code (Col. 2, lines 33-35) or into the net-list (Col.3, lines 18-20) in an automatic way (Fig. 3, EDA (Electronic Design Automation)) so that the necessary information (with which one or more post-1st verification runs as the back-stage verification can be executed against one or more design objects in the said design code or in the design net-list) can be collected during the 1st verification run (Col. 7, lines 4-11), which is the front-stage

verification, and the said one or more post-1st verification runs are executed fast" (Col. 3, lines 41-44).

Regarding claim 136, Rajsuman discloses "a design verification apparatus (Title, Abstract) comprising: a verification software and at least one or more verification platforms, wherein the said verification software instruments an additional code or a circuit into the design code (Col. 2, lines 33-35) or into the net-list (Col.3, lines 18-20) in an automatic way (Fig. 3, EDA (Electronic Design Automation)) so that dynamic information can be collected during one or more verification runs (simulation runs or simulation acceleration runs) (Col. 4, lines 33-35), and the said dynamic information collected is re-used at the post-debugging simulation after at least one design object is changed for debugging (Col. 11, lines 38-41), thereby entirely or partially reducing total verification time" (Col. 11, lines 26-28).

Regarding claim 137, Rajsuman discloses "a design verification method comprising: by using a verification software and at least one or more verification platforms the additional code or circuit is instrumented into the design code (Col. 2, lines 33-35) or into the design net-list (Col.3, lines 18-20) in an automatic way (Fig. 3, EDA (Electronic Design Automation)) so that dynamic information can be collected during one or more verification runs(simulation runs or simulation acceleration runs), and the collected dynamic information is re-used at the post-debugging simulation after at least

one design object is changed for debugging (Col. 11, lines 38-41), thereby entirely or partially reducing total verification time" (Col. 11, lines 26-28).

Regarding claim 138, this claim being dependant on claim 137 inherits the rejections of the limitations of that claim. Applicant's attention is directed to the rejection of claim 137. In addition, Rajsuman discloses "a design verification method according to claim 137, wherein the detection method of finding verification time in the case when the verification result of at least one design object changed for debugging differs from the verification result of the said design object before the change (Col. 11, lines 30-38), includes to compare either all values of outputs and inouts of the said design object before and after the change (Col. 11, lines 38-41), or compare all values of outputs of the said design object before and after the change in an automatic way, or to apply the re-simulation input stimuli(input information for replay), obtained in one or more verification runs(simulation runs or simulation acceleration runs) before modification, to the said changed design object in an automatic way, or to compare either all values of outputs and inouts of the said design object before and after the change or compare all values of outputs of the said design object before and after the change, and to apply the re-simulation input stimuli(input information for replay), obtained in one or more verification runs(simulation runs or simulation acceleration runs) before modification (Col. 8, lines 6-8), to the said changed design object in an automatic way (Col. 9, lines 28-31).

Regarding claim 139, this claim being dependant on claim 137 inherits the rejections of the limitations of that claim. Applicant's attention is directed to the rejection of claim 137. In addition, Rajsuman discloses "a design verification method according to claim 137, wherein the verification run(simulation run or simulation acceleration run), after at least one design object has been modified, is executed only either with the said at least one design object changed for debugging and its re-execution input stimuli or with the said at least one design object changed for debugging, its re-execution input stimuli(input information for replay) and only the part of design objects unchanged at least up to the first verification time when the verification result of at least one design object changed for debugging differs from the verification result of the said design object before the change from the verification time 0" (Col. 8, lines 6-15).

Regarding claim 140, this claim being dependant on claim 137 inherits the rejections of the limitations of that claim. Applicant's attention is directed to the rejection of claim 137. In addition, Rajsuman discloses "a design verification method according to claim 137, wherein the verification run(simulation run or simulation acceleration run), after at least one design object has been modified, is executed with all the design objects after the first time when the verification result of at least one design object changed for debugging differs from the verification result of the said design object before the change in an automatic way" (Col. 9, lines 28-31).

Regarding claim 141, this claim being dependant on claim 137 inherits the rejections of the limitations of that claim. Applicant's attention is directed to the rejection of claim 137. In addition, Rajsuman discloses "a design verification method according to claim 137, wherein the verification run(simulation run or simulation acceleration run), after at least one design object has been modified, is executed with all the design objects from the time, when the verification result of at least one design object changed for debugging differs from the verification result of the said design object before the change, to the time when the verification result of at least one design object changed for debugging becomes same as the verification result of the said design object before the change in an automatic way" (Col. 7, lines 26-32).

Regarding claim 142, this claim being dependant on claim 137 inherits the rejections of the limitations of that claim. Applicant's attention is directed to the rejection of claim 137. In addition, Rajsuman discloses "a design verification method according to claim 137, wherein the verification run(simulation run or simulation acceleration run) after at least one design object has been modified is executed only with the said at least one design object changed for debugging and its re-execution input stimuli(input information for replay) at least to the first verification time when the verification result of at least one design object changed for debugging differs from the verification result of the said design object before the change from the verification time 0 and after the first verification time of different results the verification run(simulation run or simulation

acceleration run) is automatically switched to the verification execution with the entire design" (Col. 8, lines 6-15).

Regarding claim 143, this claim being dependant on claim 140 inherits the rejections of the limitations of that claim. Applicant's attention is directed to the rejection of claim 140. In addition, Rajsuman discloses "a design verification method according to claim 140, or claim 142, wherein the verification run(simulation run or simulation acceleration run) with all the design objects at the said first verification time of different results, the restoring design states for the unchanged design objects occurs with the design state information saved during the verification runs(simulation runs or simulation acceleration runs) before the modification for debugging at the particular design checkpoint, which is no later than the said first verification time of different results" (Col. 11, lines 58-62).

Regarding claim 144, this claim being dependant on claim 140 inherits the rejections of the limitations of that claim. Applicant's attention is directed to the rejection of claim 140. In addition, Rajsuman discloses "a design verification method according to claim 140, or claim 142, wherein the verification run(simulation run or simulation acceleration run) with all the design objects at the said first verification time of different results, the restoring design states for the unchanged design objects occurs with the design state information saved during the verification runs(simulation runs or simulation acceleration runs) before the modification for debugging at the particular design

checkpoint, which is no later than the said first verification time of different results and be the closest one to the said first verification time of different results" (Col. 11, lines 58-62).

Regarding claim 145, this claim being dependant on claim 142 inherits the rejections of the limitations of that claim. Applicant's attention is directed to the rejection of claim 142. In addition, Rajsuman discloses "a design verification method according to claim 142, wherein the verification run(simulation run or simulation acceleration run) after design code modification, the said alignment of the dynamic information of design objects unmodified and modified at the said switching time during the verification run(simulation run or simulation acceleration run) after design code modification, or the said verification run(simulation run or simulation acceleration run) with all design objects after the said switching time after design code modification, is automatically determined by the instrumented code, which is added to the design object, during the verification run(simulation run or simulation acceleration run)" (Col. 9, lines 53-58).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to ANISS CHAD whose telephone number is (571)270-3832. The examiner can normally be reached on Monday-Thursday, 9-4 PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Frantz Coby can be reached on (571)272-4017. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

ANISS CHAD
Examiner
Art Unit 4191

/A. C./
Examiner, Art Unit 4191

/Nabil El-Hady/

Supervisory Patent Examiner, Art Unit 4191